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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title : COMB FILTER SYSTEM FOR DECIMATING A SEQUENCE OF DIGITAL INPUT VALUES TO A SEQUENCE OF DIGITAL OUTPUT VALUES BY A NON-INTEGER FACTOR

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to examination, amend the application as follows:

In the claims:

Cancel claims 1-7.

Add claims 8-26:

-- 8. An arrangement for decimating an input value, the arrangement comprising:

an integrator that outputs the input value to a signal path, the signal path including;

a delay stage configured to adjust the input value using a delay factor;

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a decimator configured to convert the input value into a decimated output value using a non-integral factor;

a differentiator configured to generate an intermediate output value from the input value; and

an interpolation arrangement configured to receive the intermediate output value and generates a decimated sequence of the output value.

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